WHAT IS CLAIMED IS:

1. An N-bit analog to digital converter (ADC) comprising:

a reference ladder;

a track-and-hold amplifier tracking an input voltage with its output;

a coarse ADC amplifier connected to a coarse capacitor at its input and having a coarse ADC reset switch controlled by a first clock phase of a two-phase clock;

a fine ADC amplifier connected to a fine capacitor at its input and having a fine ADC reset switch controlled by a second clock phase of the two-phase clock, wherein the track-and-hold amplifier is in a hold-mode during the second clock phase;

a switch matrix that selects a voltage subrange from the reference ladder for use by the fine ADC amplifier based on an output of the coarse ADC amplifier,

wherein the coarse capacitor is charged to a coarse reference ladder voltage during the first clock phase and connected to the T/H output voltage during the second clock phase, and

wherein the fine capacitor is connected to a voltage subrange during the first clock phase and charged to the track-and-hold output voltage during the second clock phase; and

an encoder that converts outputs of the coarse and fine ADC amplifiers to an N-bit output.

2. The analog to digital converter of claim 1, wherein the coarse ADC reset switch is a field effect transistor (FET).

3. The analog to digital converter of claim 1, wherein the first and second clock phases are non-overlapping.

4. The analog to digital converter of claim 1, wherein the fine ADC amplifier includes a plurality of cascaded amplifier stages.

5. The analog to digital converter of claim 1, wherein the coarse ADC amplifier includes a plurality of cascaded amplifier stages.

6. The analog to digital converter of claim 1, wherein the coarse capacitor is connected to the track-and-hold amplifier output on a delayed second phase.

7. The analog to digital converter of claim 1, wherein the fine ADC capacitor is connected to the track-and-hold amplifier output on a delayed second clock phase and to the voltage subrange during a delayed first clock phase.

8. The analog to digital converter of claim 1, further including a switch that connects an output of the track-and-hold-amplifier to the coarse capacitor on the second clock phase.

9. The analog to digital converter of claim 1, further including a coarse comparator that latches the output of the coarse ADC amplifier and outputs it to the encoder.

10. The analog to digital converter of claim 1, further including a fine comparator that latches the output of the fine ADC amplifier and outputs it to the encoder.

11. An N-bit analog to digital converter comprising:

a reference ladder;

a track-and-hold amplifier tracking an input voltage;

a two-phase clock having phases φ_1 and φ_2;

a plurality of coarse ADC amplifiers each connected to a corresponding coarse capacitor at its input, wherein the coarse ADC amplifiers are reset on φ_1 and their corresponding coarse capacitors are connected to an output of the track-and-hold on φ_2, and wherein the track-and-hold amplifier is in a hold-mode on φ_2;

a plurality of fine ADC amplifiers each connected to a corresponding fine capacitor at its input, wherein the fine ADC amplifiers are reset on φ_2 and their corresponding fine capacitors are charged to the track-and-hold amplifier output voltage on φ_2;

a switch matrix that selects a voltage subrange from the reference ladder, based on outputs of the coarse ADC amplifiers, for input to the fine ADC amplifiers on φ_1; and

an encoder that converts outputs of the coarse and fine ADC amplifiers to an N-bit output.

12. The analog to digital converter of claim 11, further including a FET switch that resets the coarse ADC amplifier on φ_1.

13. The analog to digital converter of claim 11, wherein the φ_1 and φ_2 phases are non-overlapping.

14. The analog to digital converter of claim 11, wherein the fine ADC amplifiers include a plurality of cascaded amplifier stages.

15. The analog to digital converter of claim 11, wherein the coarse ADC amplifiers include a plurality of cascaded amplifier stages.

16. The analog to digital converter of claim 11, wherein the coarse capacitors are connected to the track-and-hold amplifier output on a delayed φ_2.

17. The analog to digital converter of claim 11, wherein the fine capacitors are connected to the track-and-hold amplifier output on a delayed φ_2, and to the voltage subrange on a delayed φ_1.

18. The analog to digital converter of claim 11, further including switches that connect an output of the track-and-hold to the coarse capacitors on φ_2.

19. The analog to digital converter of claim 11, further including a plurality of coarse comparators that latch the outputs of the coarse ADC amplifiers and output them to the encoder.

20. The analog to digital converter of claim 11, further including a plurality of fine comparators that latch the outputs of the fine ADC amplifiers and output them to the encoder.

21. An N-bit analog to digital converter comprising:

a reference ladder;

a track-and-hold amplifier tracking an input voltage;

a two-phase clock having phases φ_1 and φ_2;

a coarse capacitor connected to the track-and-hold amplifier on φ_2 and to the reference ladder on φ_1;

a coarse ADC amplifier that resets on φ_1 and amplifies a voltage on the coarse capacitor on φ_2;

a coarse comparator for latching an output of the coarse ADC amplifier on $\varphi_{1+1\ cycle}$;

a fine capacitor connected to the track-and-hold on φ_2 and to a fine voltage tap of the reference ladder on φ_1, the fine voltage tap selected based on the output of the coarse ADC amplifier, wherein the track-and-hold amplifier is in a hold-mode on φ_2;

a fine ADC amplifier including a plurality of cascaded amplifier stages,

wherein a first cascaded amplifier stage resets on φ_2 and amplifies a voltage on the fine capacitor on $\varphi_{1+1cycle}$, a second cascaded amplifier stage resets on $\varphi_{1+1cycle}$ and amplifies the voltage on the fine capacitor on $\varphi_{2+1\ cycle}$, a third cascaded amplifier stage resets on $\varphi_{2+1cycle}$ and amplifies the voltage on the fine capacitor on $\varphi_{1+2\ cycles}$, and so on;

a fine comparator for latching an output of a last cascaded amplifier stage; and

an encoder converting outputs of the coarse and fine comparators to an N-bit output.

22. The analog to digital converter of claim 21, wherein the phases φ_1 and φ_2 are non-overlapping.

23. The analog to digital converter of claim 21, wherein the coarse capacitor connects to the track-and-hold on a delayed φ_2.

24. The analog to digital converter of claim 21, wherein the fine ADC capacitor is connected to the track-and-hold on a delayed φ_2 and to the fine voltage tap on a delayed φ_1.

25. The analog to digital converter of claim 21, further including a FET switch that connects the track-and-hold amplifier to the coarse capacitor on φ_2.

26. The analog to digital converter of claim 21, further including a coarse comparator that latches the output of the coarse ADC amplifier and outputs it to the encoder.

27. The analog to digital converter of claim 21, further including a fine comparator that latches the output of the fine ADC amplifier and outputs it to the encoder.

28. An N-bit analog to digital converter comprising:

a reference ladder;

a track-and-hold amplifier tracking an input voltage;

a two-phase clock having alternating phases φ_1 and φ_2;

a plurality of coarse capacitors connected to an output of the track-and-hold on φ_2 and to corresponding coarse taps of the reference ladder on φ_1;

a plurality of coarse ADC amplifiers that reset on φ_1 and amplify voltages on the coarse capacitors on φ_2;

a plurality of coarse comparators for latching outputs of the coarse ADC amplifiers;

a plurality of fine capacitors connected to the output of track-and-hold amplifier on φ_2 and connected to fine voltage taps of the reference ladder on φ_1, the fine voltage taps selected based on the outputs of the coarse ADC amplifiers, wherein the track-and-hold amplifier is in a hold-mode on φ_2;

a plurality of fine ADC amplifiers, each including a plurality of cascaded amplifier stages,

wherein the cascaded amplifier stages reset and amplify on alternating phases φ_1 and φ_2,

wherein amplifiers of the first stage are reset on φ_2 and amplify voltages of the fine capacitors on φ_1;

a plurality of fine comparators for latching outputs of a last amplifier stage; and

an encoder converting outputs of the coarse and fine comparators to an N-bit output.

29. The analog to digital converter of claim 28, wherein the φ_1 and φ_2 phases are non-overlapping.

30. The analog to digital converter of claim 28, wherein the fine capacitors are connected to the output of the track-and-hold amplifier during a delayed φ_2 and to the fine voltage taps on a delayed φ_1.

31. The analog to digital converter of claim 28, further including a plurality of switches that connect the output of the track-and-hold to the coarse capacitors on φ_2.

32. An N-bit analog to digital converter comprising:

a two-phase clock having phases φ_1 and φ_2;

a reference ladder;

a track-and-hold amplifier tracking an input voltage;

a coarse ADC amplifier that resets on φ_1 and amplifies a difference of an output of the track-and-hold amplifier and a coarse tap of the reference ladder on φ_2, wherein the track-and-hold amplifier is in a hold-mode on φ_2;

a fine ADC amplifier that resets on φ_2 and amplifies a difference of the output of the track-and-hold amplifier and a fine tap of the reference ladder on φ_1;

a switch matrix that selects a voltage subrange from the reference ladder for use by the fine ADC amplifier based on an output of the coarse ADC amplifier; and

an encoder that converts outputs of the coarse and fine ADC amplifiers to an N-bit output.

33. A method of converting analog to digital voltage comprising the steps of:

resetting a coarse ADC amplifier on the first clock phase;

charging a coarse capacitor to a first reference voltage during a first clock phase of a two phase clock;

connecting the coarse capacitor to an input voltage during a second clock phase of the two phase clock;

wherein the T/H amplifier is in hold-mode during the 2nd clock phase;

selecting the second reference voltage based on an output of the coarse ADC amplifier;

connecting a fine capacitor to a second reference voltage during the first clock phase;

charging the fine capacitor to the input voltage during the second clock phase;

amplifying a voltage on the coarse capacitor on the second clock phase;

resetting a fine ADC amplifier on the second clock phase;

amplifying a voltage of the fine capacitor on the first clock phase; and

converting outputs of the coarse and fine ADC amplifiers to an N-bit output.

34. A method of converting analog to digital voltage comprising the steps of:

on a first clock phase, charging a coarse capacitor to a first reference voltage, connecting a fine capacitor to a second reference voltage, resetting a coarse ADC amplifier, and amplifying a voltage of the fine capacitor;

on a second clock phase, connecting the coarse capacitor to an output of a track-and-hold amplifier, setting the track-and-hold amplifier to a hold mode, charging the fine capacitor to the input voltage, resetting a fine ADC amplifier, selecting a voltage subrange from the reference ladder for use by the fine ADC amplifier based on an output of the coarse ADC amplifier; and

converting outputs of the coarse and fine ADC amplifiers to an N-bit output.